WHAT IS CLAIMED IS:

1. A semiconductor package comprising:

a semiconductor die;

a leadframe attached to the die; and

a molded plastic body comprising an inner member on the leadframe, and an outer member substantially encapsulating the inner member;

the inner member dimensioned such that the outer member comprises substantially equal volumes of a molding compound on either side of the leadframe.

2. The semiconductor package of claim 1 wherein the inner member substantially encapsulates the die and a portion of the leadframe proximate to the die.

3. The semiconductor package of claim 1 wherein the inner member comprises the molding compound.

4. The semiconductor package of claim 1 wherein the inner member comprises a polymer deposited on the leadframe.

5. The semiconductor package of claim 1 wherein the inner member comprises a polymer tape attached to the leadframe.

6. A semiconductor package comprising:

a semiconductor die;

a leadframe having a first side wire bonded to the die and a second side attached to the die;

an inner member attached to the first side or to the second side of the leadframe and configured to rigidify the package; and

a plastic body comprising a molding compound substantially encapsulating the die, the wire bonds, the inner member, and at least a portion of the leadframe;

the plastic body and the inner member dimensioned such that there are substantially equal volumes of the molding compound on either side of the leadframe.

7. The semiconductor package of claim 6 wherein the inner member comprises the molding compound.

8. The semiconductor package of claim 6 wherein the inner member comprises a separate member attached to the second side of the leadframe.

9. The semiconductor package of claim 6 wherein the inner member comprises a glob top polymer on the second side of the leadframe.

10. The semiconductor package of claim 6 wherein the inner member comprises a polymer tape attached to the leadframe.

11. The semiconductor package of claim 6 wherein the inner member comprises a second molding compound substantially encapsulating the die.

12. A semiconductor package comprising:

a semiconductor die;

a leadframe comprising a plurality of terminal leads in electrical communication with the die; and

a plastic body comprising a molded inner member substantially encapsulating the die and a first portion of the leadframe, and a molded outer member comprising a molding

compound substantially encapsulating the inner member and a second portion of the leadframe;

the inner member configured to rigidify the package and to prevent bowing of the plastic body during cooling of the molding compound.

13. The semiconductor package of claim 12 wherein the molded inner member comprises the molding compound.

14. The semiconductor package of claim 12 wherein the molded inner member has a geometrical configuration selected such that the molded outer member comprises substantially equal volumes of the molding compound on either side of the leadframe.

15. A semiconductor package comprising:

a semiconductor die;

a leadframe attached to the die having a first side and a second side and comprising a plurality of terminal leads electrically connected to the die; and

a plastic body comprising an inner member encapsulating the die and a first portion of the leadframe proximate to the die, and an outer member encapsulating the inner member and a second portion of the leadframe proximate to the terminal leads, the inner member dimensioned such that the outer member comprises substantially equal volumes of a molding compound on either side of the leadframe.

16. The package of claim 15 wherein the inner member and the outer member comprise a same molding compound.

17. The package of claim 15 wherein the leadframe comprises a plurality of leadfingers attached to the die.

18. The package of claim 15 further comprising a plurality of wire bonds bonded to the leadframe and to the die and substantially encapsulated by the inner member.

19. The package of claim 15 wherein the die and the leadframe have a lead on chip (LOC) configuration.

20. The package of claim 15 wherein the package comprises a thin small outline package (TSOP).

21. A semiconductor package comprising:

a semiconductor die comprising a face and a plurality of bond pads on the face;

a leadframe comprising a plurality of leadfingers having first sides attached to the face of the die and second sides;

a plurality of wire bonds bonded to the bond pads and to the second sides of the lead fingers;

a plastic body comprising:

a molded inner member comprising a molding compound substantially encapsulating the die, the wire bonds, and the leadfingers;

a molded outer member comprising the molding compound substantially encapsulating the molded inner member;

the molded inner member and the molded outer member dimensioned such that the molded outer member comprises substantially equal volumes of the molding compound on either side of the leadframe.

22. The semiconductor package of claim 21 wherein the package comprises a thin small outline package (TSOP).

23. The semiconductor package of claim 21 wherein the die and the leadframe have a lead on chip (LOC) configuration.

24. The semiconductor package of claim 21 wherein the leadfingers comprise a plurality of substantially planar terminal leads projecting from the plastic body.

25. The semiconductor package of claim 21 wherein the leadfingers comprise a plurality of terminal leads projecting from the plastic body and having an offset relative to one another of less than about 3 mils.

26. A semiconductor package comprising:

a semiconductor die;

a leadframe attached to the die; and

a molded plastic body substantially encapsulating the die and at least a portion of the leadframe;

a volume equalizing member attached to the leadframe configured to rigidify the package and dimensioned such that the molded plastic body comprises substantially equal volumes of a molding compound on either side of the leadframe.

27. The semiconductor package of claim 26 wherein the volume equalizing member comprises a molded inner member comprising a second molding compound.

28. The semiconductor package of claim 26 wherein the volume equalizing member comprises a glob top polymer deposited on the leadframe.

29. The semiconductor package of claim 26 wherein the volume equalizing member comprises a polymer tape attached to the leadframe.

30. A method for fabricating a semiconductor package comprising:

providing a leadframe;

providing a semiconductor die;

attaching the die to the leadframe;

forming an inner member on the leadframe configured to rigidify and prevent bowing of the package;

molding a package body on the inner member, on the die and on at least a portion of the leadframe;

the inner member and the package body dimensioned such that the package body comprises substantially equal volumes of a molding compound on either side of the leadframe.

31. The method of claim 30 wherein forming the inner member comprises molding a second molding compound on the die and at least a portion of the leadframe.

32. The method of claim 30 wherein forming the inner member comprises depositing a glob top polymer on the leadframe.

33. The method of claim 30 wherein forming the inner member comprises attaching a polymer tape to the leadframe.

34. A method for fabricating a semiconductor package comprising:

providing a leadframe and a semiconductor die attached to the leadframe;

providing a first molding cavity;

molding an inner member on the die and the leadframe using the first molding cavity;

providing a second molding cavity;

molding an outer member on the inner member, and on at least a portion of the leadframe using the second molding cavity.

35. The method of claim 34 wherein the inner member and the outer member are dimensioned such that the outer member comprises substantially equal volumes of a molding compound on either side of the leadframe.

36. The method of claim 34 wherein the inner member and the outer member comprise a same molding compound.

37. A method for fabricating a semiconductor package comprising:

providing a leadframe;

attaching a semiconductor die to the leadframe;

forming a plastic body on the die and the leadframe using a two stage encapsulation process comprising:

molding an inner member on the die and the leadframe in a first stage, the inner member substantially encapsulating the die;

molding an outer member on the inner member and at least a portion of the leadframe in a second stage, the outer member and the inner member dimensioned such that the outer member comprises substantially equal volumes of a molding compound on either side of the leadframe.

38. The method of claim 37 further comprising at least partially curing the inner member prior to molding the outer member.

39. The method of claim 37 wherein molding the inner member is performed using a first mold cavity and molding the outer member is performed using a second mold cavity.

40. The method of claim 37 further comprising forming wire bonds between the die and the leadframe and

substantially encapsulating the wire bonds during molding of the inner member.

41. The method of claim 37 wherein the die and the leadframe have a lead on chip configuration.

42. The method of claim 37 wherein the package comprises a thin small outline package (TSOP).

43. A method for fabricating a semiconductor package comprising:

providing a leadframe;

providing a semiconductor die;

attaching the die to the leadframe;

forming a volume equalizing member on the leadframe;

molding a package body on the volume equalizing member, on the die and on at least a portion of the leadframe;

the package body and the volume equalizing member dimensioned such that the package body comprises substantially equal volumes of a molding compound on either side of the leadframe.

44. The method of claim 43 wherein forming the volume equalizing member comprises molding an inner member on the die.

45. The method of claim 43 wherein forming the volume equalizing member comprises depositing a glob top on the leadframe.

46. The method of claim 43 wherein forming the volume equalizing member comprises attaching a polymer tape to the leadframe.

47. A method for fabricating a semiconductor package comprising:

providing a semiconductor die;

providing a lead on chip leadframe comprising a plurality of lead fingers configured for attachment and wire bonding to the die;

attaching the lead fingers to the die;

forming wire bonds between the lead fingers and the die;

forming a volume equalizing member by encapsulating the die, the wire bonds and first portions of the lead fingers proximate to the die in a molding compound;

at least partially curing the molding compound;

forming a plastic body on the volume equalizing member by encapsulating the volume equalizing member and second portions of the lead fingers; and

selecting a geometry of the volume equalizing member such that the plastic body comprises substantially equal volumes of the molding compound on either side of the leadframe.

48. The method of claim 47 wherein forming the volume equalizing member is performed using a first mold cavity.

49. The method of claim 47 wherein forming the plastic body is performed using a second mold cavity.

50. The method of claim 47 wherein the package comprises a thin small outline package (TSOP).

51. An electronic assembly comprising:

a substrate comprising a plurality of electrodes;

a plastic semiconductor package on the substrate comprising:

a semiconductor die;

a leadframe comprising a plurality of terminal leads in electrical communication with the die and bonded to the electrodes; and

a plastic body comprising a molded inner member substantially encapsulating the die and a first portion of the leadframe, and a molded outer member comprising a molding compound substantially encapsulating the inner member and a second portion of the leadframe;

the inner member configured to substantially equalize a volume of the molding compound on either side of the leadframe.

52. The assembly of claim 51 wherein the molded inner member comprises the molding compound.

53. The assembly of claim 51 wherein the substrate comprises a circuit board.

54. The assembly of claim 51 wherein the assembly comprises a multi chip module.

55. An electronic assembly comprising:

a substrate comprising a plurality of electrodes;

a plastic semiconductor package on the substrate comprising:

a semiconductor die;

a leadframe attached to the die and comprising a plurality of terminal leads bonded to the electrodes;

a molded plastic body substantially encapsulating the die and at least a portion of the leadframe;

a volume equalizing member attached to the leadframe configured to rigidify the package and dimensioned such that the molded plastic body comprises substantially

equal volumes of a molding compound on either side of the leadframe.

56. The assembly of claim 55 wherein the volume equalizing member comprises a glob top polymer or a polymer tape.